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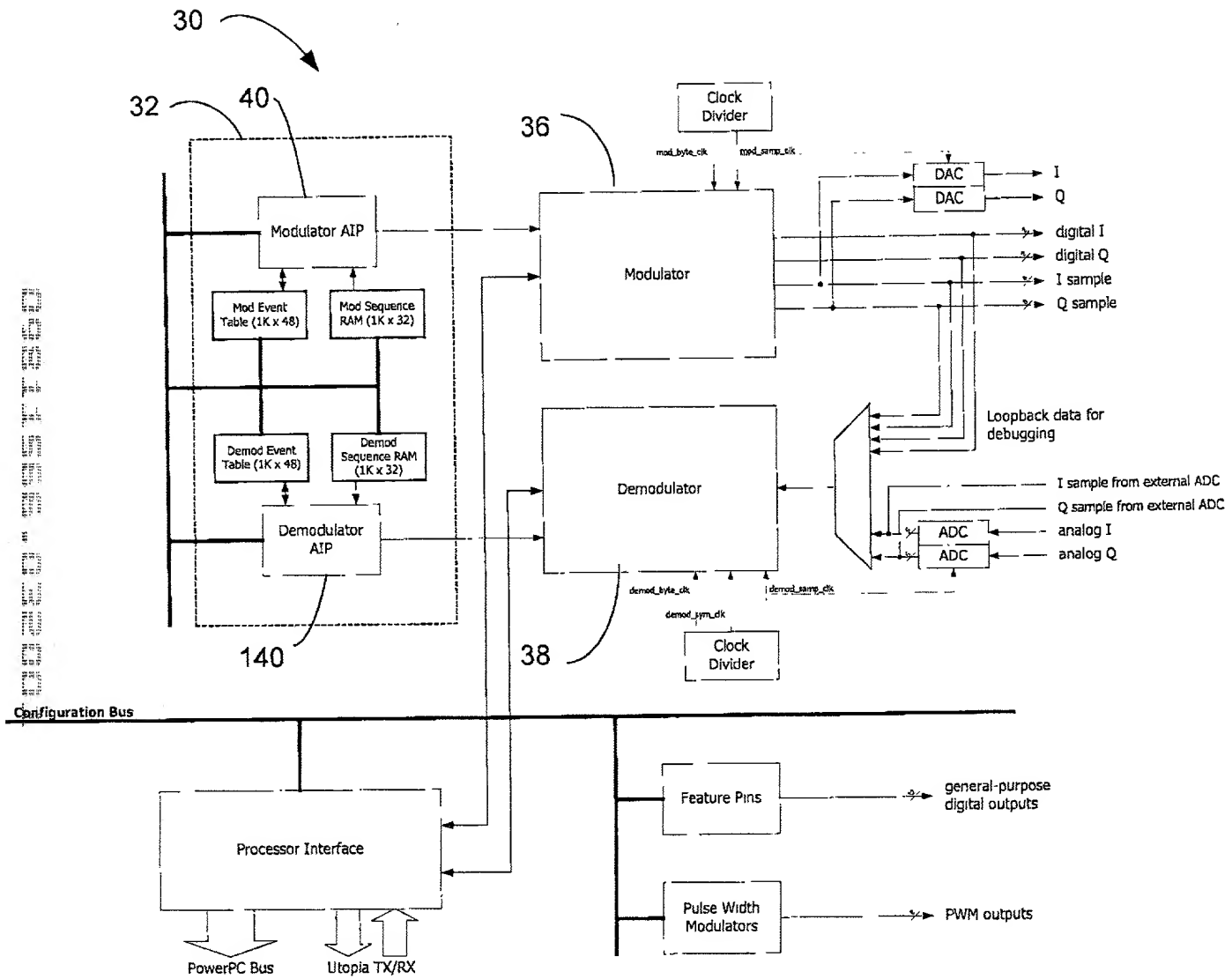


Figure 1

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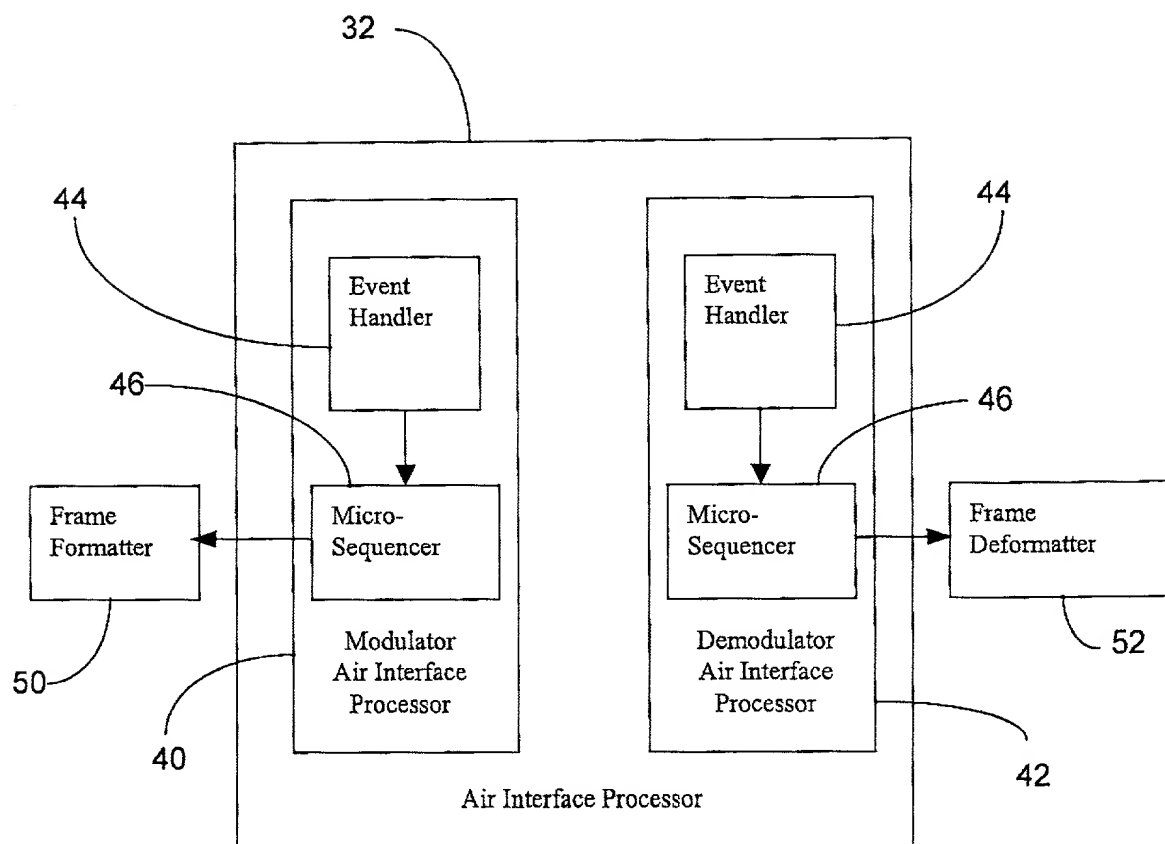


Figure 2

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Instruction	44444444	33333333	22222222	11111111	00000000	76543210	98765432	10987654	32109876	54321098	76543210
Type 1	00	ALU opcode	SW Rd	Rn	operand 2	branch code	pass address	fail address			
Type 2	0100	Rhi	-	Rlo	32-bit data						
Type 3	0101	Rhi	Imm_lo		32-bit data						
Type 4	0110	Rhi	-	Rlo	-						Rd
Type 5	0111	Rhi	Imm_lo		-						Rd
Type 6	1TDQ	0	Microsequence r address		trigger time						
Type 7	1	-	01	-	burst info						
Type 8	1	-	A11	-					mask		

Instruction Type 1: ALU Operations
 Instruction Type 2: Write register
 Instruction Type 3: Write register immediate
 Instruction Type 4: Read register
 Instruction Type 5: Read register immediate
 Instruction Type 6: Trigger
 Instruction Type 7: BURST
 Instruction Type 8: WAIT
 [A='0' → until any of (R12 and mask) bits are set]
 [A='1' → until all of (R12 and mask) bits are set]

Figure 3: Event Handler Instruction Set Summary

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[illegible]

Figure 4: Register Access Instructions

[illegible]

Figure 5: Data Scheduling Instructions

[illegible]

Figure 6: Burst Descriptor Instruction

33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
PS		value to DDS/Fractional-N counter																																

Figure 7: Modulator Burst Info Field Format

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
User ID														PS		Expected Length														

Figure 8: Demodulator Burst Info Field Format

[illegible]

Figure 9: Processor Wait Instruction

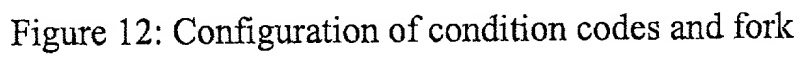
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opcode	name	Description
00000	JZ	Jump to Zero
00001	CJS	Conditional Jump to Subroutine
00010	JMAP	Jump Map
00011	CJP	Conditional Jump Pipeline
00100	PUSH	Push/Conditional Load Counter
00101	JSRP	Conditional Jump to Subroutine
00110	CJV	Conditional Jump Vector
00111	JRP	Conditional Jump
01000	RFCT	Repeat Loop Counter Not Equal to Zero
01001	RPCT	Repeat Pipeline Counter Not Equal to Zero
01010	CRTN	Conditional Return
01011	CJPP	Conditional Jump Pipeline and Pop
01100	LDCT	Load Counter and Continue
01101	LOOP	Test End of Loop
01110	CONT	Continue
01111	TWB	Three Way Branch
10000	FORK	Multiway Branch
others		reserved

Figure 10: Microsequencer Instruction Set

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OPCODE								EMIT								CCSEL				CP	FFCMD						SB	OC	-	SR	

Figure 11: Microsequencer memory format

[illegible]

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1	x	x	1	x	Match	
0	0	0	0	0	0	0
0	0	0	0	1	0	
0	0	0	1	0	0	
0	0	0	1	1	0	
0	0	1	0	0	0	0
0	0	1	0	1	0	
0	0	1	1	0	0	
0	0	1	1	1	0	
0	1	0	0	0	0	0
0	1	0	0	1	0	
0	1	0	1	0	0	
0	1	0	1	1	0	
0	1	1	0	0	0	0
0	1	1	0	1	0	
0	1	1	1	0	0	
0	1	1	1	1	0	
1	0	0	0	0	0	C
1	0	0	0	1	0	
1	0	0	1	0	1	
1	0	0	1	1	1	
1	0	1	0	0	0	C
1	0	1	0	1	0	
1	0	1	1	0	1	
1	0	1	1	1	1	
1	1	0	0	0	0	C
1	1	0	0	1	0	
1	1	0	1	0	1	
1	1	0	1	1	1	
1	1	1	0	0	0	C
1	1	1	0	1	0	
1	1	1	1	0	1	
1	1	1	1	1	1	

Figure 13

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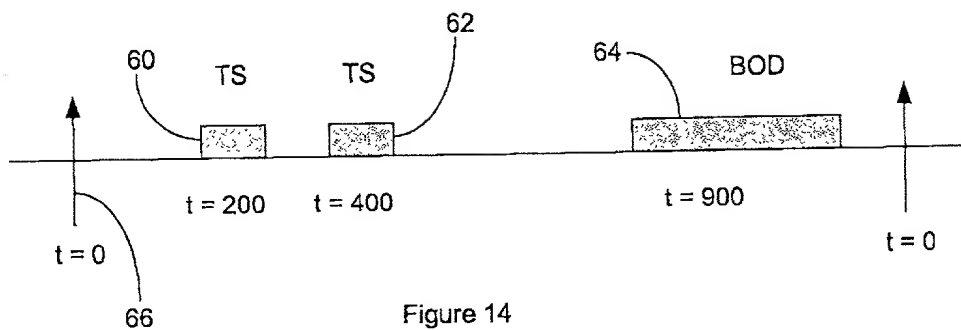


Figure 14

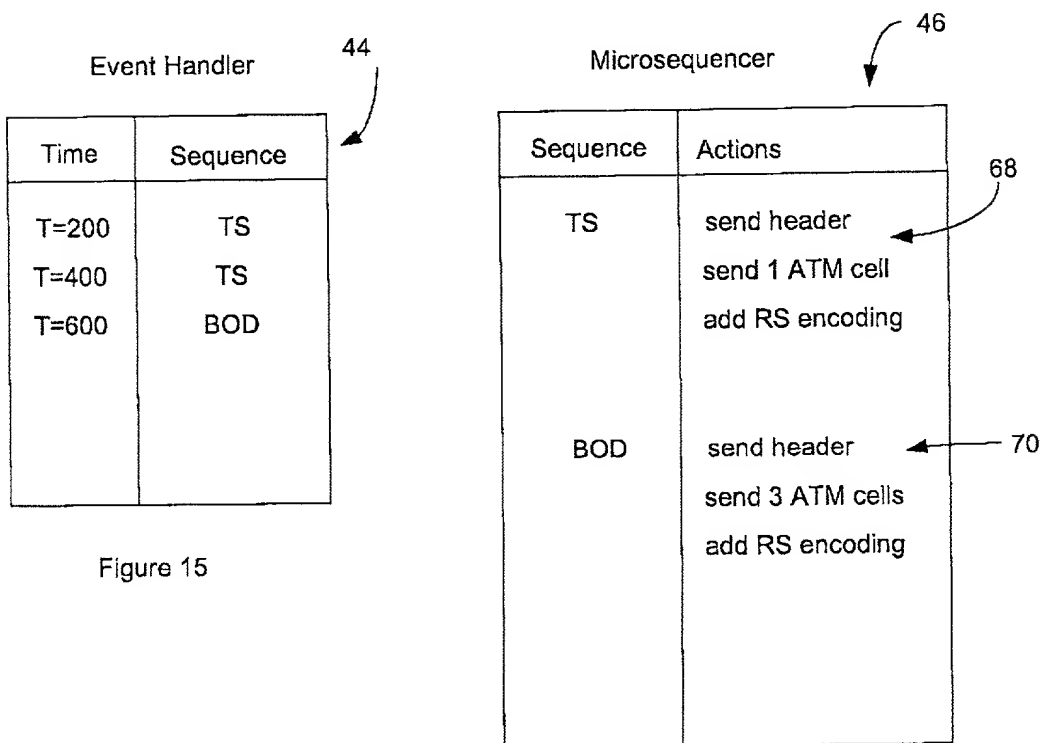


Figure 15

Figure 16

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Terminal Modulator Block Diagram

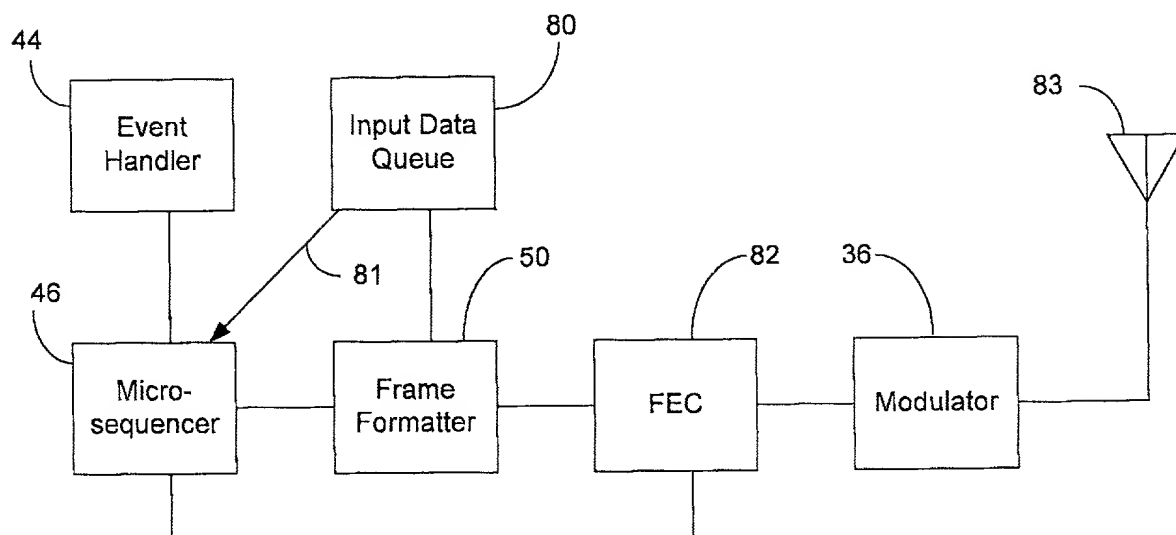


Fig 17

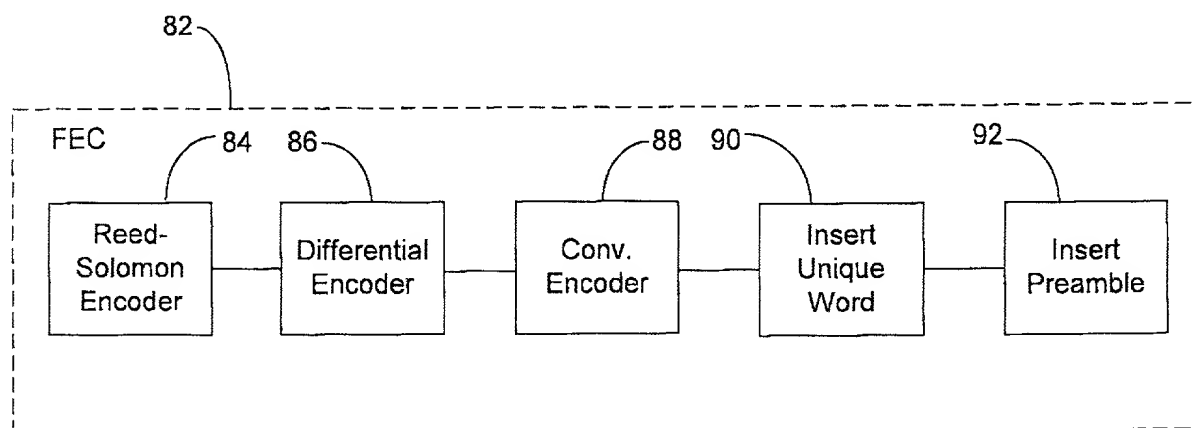


Fig 18

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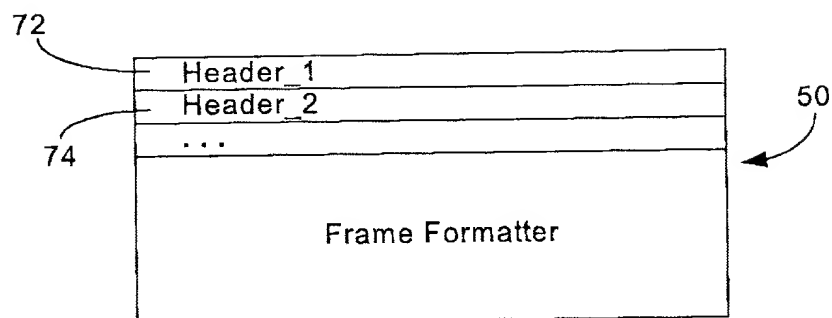


Figure 19

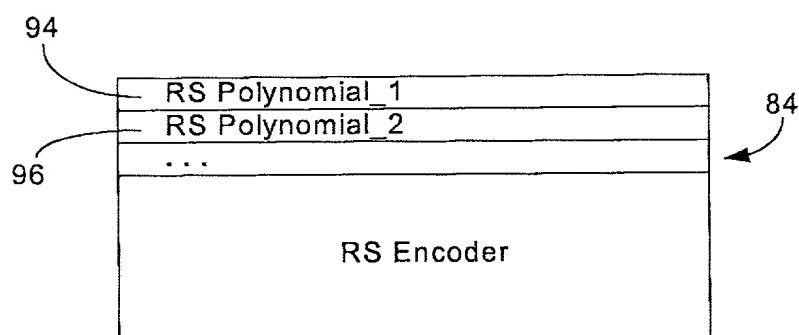


Figure 20

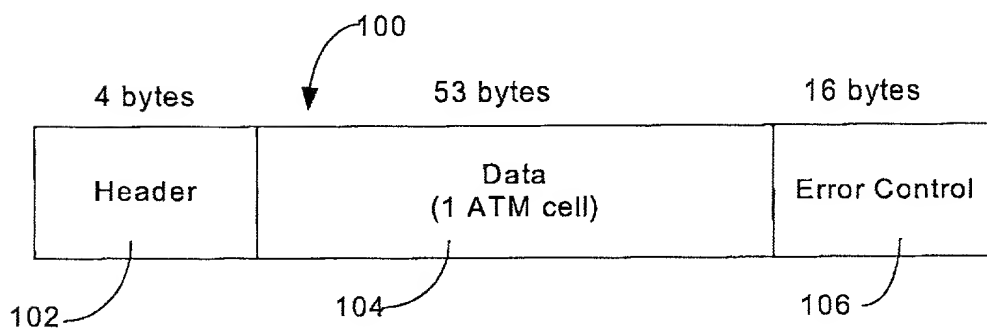


Figure 21

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Terminal Demodulator Block Diagram

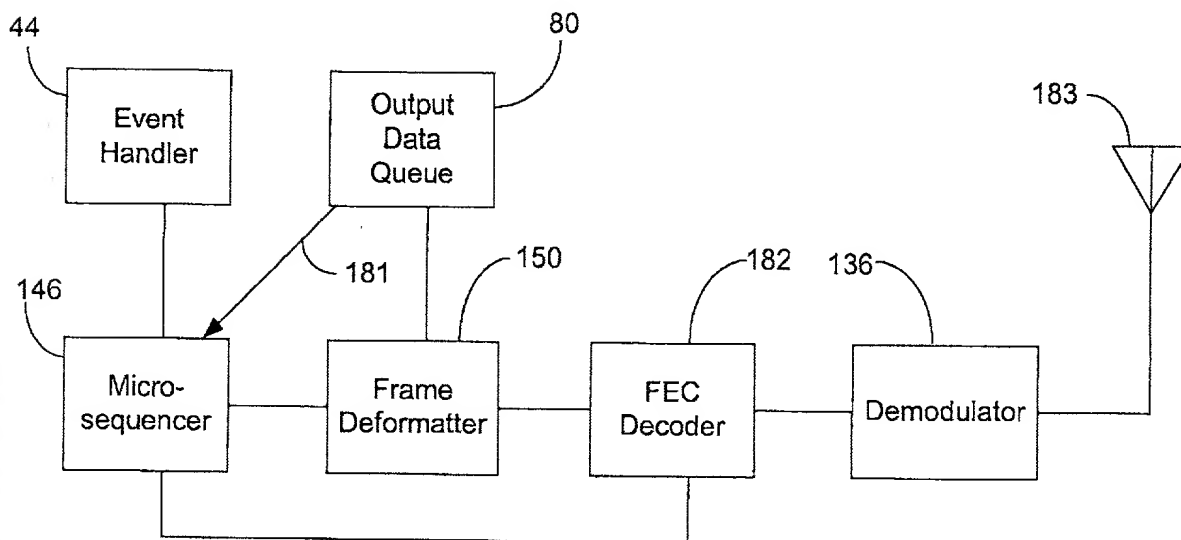


Fig 22

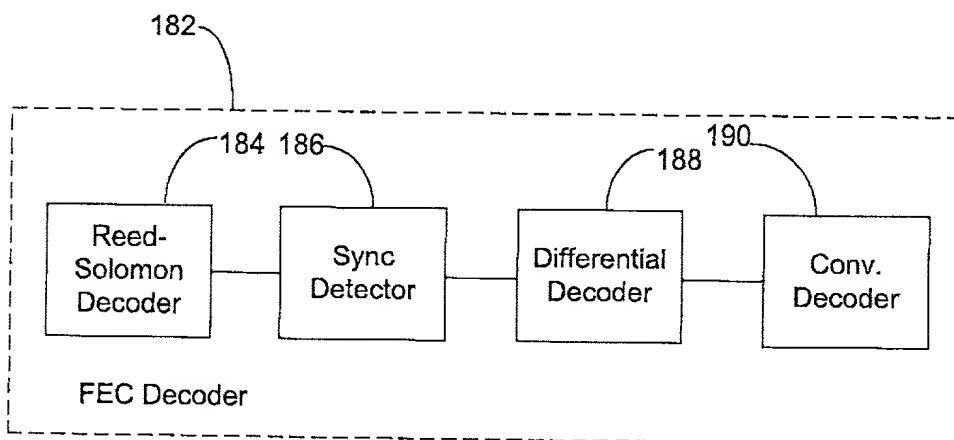


Fig 23